REMARKS

With this amendment, Applicant has amended claims 1-10 for clarity. Applicant has further added new claims 11-25 in order to claim additional aspects of the present invention. Furthermore, Applicant has amended the specification in a number of places to correct typographical errors. Upon entry of the present amendment, the pending claims will be 1-25. Finally, Applicant has replaced the abstract in view of the changes to the pending claims. No new matter has been added by way of these amendments to claims 1-10, addition of claims 11-25, changes to the specification, or by the replacement abstract.

This amendment responds to the July 13, 2004 Office Action. In the Office Action the Examiner:

- objected to claims 1-10;
- rejected claims 1 and 5 under 35 U.S.C. § 102(a) as being anticipated by Saito *et al.*, 2000, arXiv:quant-ph/0001113.1 (hereinafter "Saito");
- rejected claim 6 under 35 U.S.C. § 102(b) as being anticipated by Griffiths and Niu, 1996, Physical Review Letters 76, pp. 3228-3231 (hereinafter "Griffiths");
- rejected claims 2-4 under 35 U.S.C. § 103 as being unpatentable over Griffiths in view of Saito; and
- rejected claims 7-10 under 35 U.S.C. § 103 as being unpatentable over Griffiths in view of paragraph 036 of Applicant's specification.

THE CLAIM OBJECTIONS SHOULD BE WITHDRAWN

Claims 1-5. The Examiner has objected to claims 1-5 for allegedly failing to clarify what basic quantum circuit structure(s) the recited operations are implemented on for the recited quantum computation. Applicant has amended claim 1 to indicate that the recited operations are for implementation on a quantum computing device comprising a plurality of qubits. However, claim 1, as amended, does not require actual implementation of a first series of operations or a second series of operations on the quantum computing device. Newly added claim 19 depends from claim 1 and recites the additional step of actually executing the second series of operations on the quantum computing device thereby computing a quantum calculation.

The Examiner has further objected to claims 1-5 for allegedly failing to clarify what are the functions of the first and second series of operations. Applicant has amended claim 1 to indicate that the both the first series and second series of operations

collectively implement a quantum calculation on a quantum computing device. Moreover, Applicant has added new claim 17 to provide an example of such a quantum calculation. In claim 17, the quantum calculation is a quantum Fourier transform.

The Examiner has further objected to claims 1-5 for allegedly failing to clarify whether the claims recite a method of operating a quantum device or a method of designing a method to operate a quantum device. Applicant believes that the amendments to claim 1 make it clear that the claim encompasses a method of optimizing a series of operations. Claim 1 does not recite execution of the optimized calculations (the second series of operations) on a quantum computing device. Applicants has added new claim 19 to teach this additional step.

The Examiner has further objected to claims 1-5 for allegedly failing to clarify whether the first series of operations is actually implemented in the recited computation. Applicant has amended claim 1 to clarify that both the first series of operations and the second series of operations result in the execution of the same quantum calculation. For example, both the first series of operations and the second series of operations can implement a quantum Fourier transform on a quantum computing device. However, the second series of operations can be performed on the quantum computing device in less time then the first series of operations. Thus, the second series of operations is more desirable than the first series of operations even though both series of operations implement the same quantum calculation on the quantum computing device. Thus, Applicant believes that it is clear that there is no requirement that the first series of operations is actually implemented on the quantum computing device.

The Examiner has further objected to claims 1-5 for allegedly failing to clarify whether the recited swap operation is definitely eliminated or included in the recited method. The swap operation at issue is recited in claims 3, 4, and 5. Therefore, Applicant addresses this objection with respect to claims 3-5 only. Claim 3 merely recites that the first series of operations includes a swap operation. Applicant sees no reason to further clarify claim 3. Claims 4 and 5 have been amended to recite "omitting the swap operation from the first series of operations in order to form the second series of operations." Applicant believes that it is now clear that claims 4 and 5 recite that the swap operation is removed from the first series of operations in order to form the second series of operations.

In view of the reasons set forth above and the various claim amendments made to claims 1-5, Applicant now believes that all of the objections to claims 1-5 raised by the

Examiner have been addressed. Applicant therefore respectfully requests that the objections to claims 1-5 be withdrawn.

Claims 6-10. The Examiner has objected to claims 6-10 for allegedly failing to clarify what basic quantum circuit structure(s) the recited operations are implemented on for the recited quantum computation. Applicant has amended claim 6 to indicate that the operations are performed on a quantum computing device that comprises a plurality of qubits.

The Examiner has further objected to claims 6-10 for allegedly failing to indicate the respective functions of the recited sequence of operations. Applicant has amended claim 6 to recite that the sequence of operations collectively implement a swap operation on the quantum computing device.

The Examiner has further objected to claims 6-10 for allegedly failing to indicate the respective functions of the two operations that commute. Applicant respectfully disagrees with this objection. The specification provides ample support and examples of the functions of two operations that commute and therefore can be performed on different qubits simultaneously. See, for example, paragraph 41 of the specification. In particular, see the description of the operations (gates) blocked off by square brackets in Equation 13 that are described at the end of paragraph 41 of the specification.

The Examiner has further objected to claims 6-10 for allegedly failing to clarify how the recited two operations can be performed simultaneously when they are already defined as sequenced and complete operations in the recited sequence of operations. Applicant has amended claim 6 so that it is now clear that the two operations are performed simultaneously on different qubits. Applicant believes that the claim language of claims 6-10 does not preclude a series of operations from including two operations that are performed simultaneously.

The Examiner has further objected to claim 6-10 allegedly failing to clarify the exact definition of Z, X and CP. Applicant has provided description of these operators in the specification. See, for example, paragraphs 35-37 of the specification. These operators are well known in the art and have been described in two publications that have been incorporated by reference in the instant application (see the references cited in paragraph 36 of the specification). However, Applicant in no way relies on these incorporated references to support the definitions of Z, X and CP because the operators are well known art recognized operators.

The Examiner has also objected to claim 10 because it depends from an incorrect claim. Applicant has fixed the dependency of claim 10. Amended claim 10 now depends from claim 7.

In view of the reasons set forth above and the various claim amendments made to claims 6-10, Applicant now believes that all of the objections to claim 6-10 raised by the Examiner have been addressed. Applicant therefore respectfully requests that the objections to claims 6-10 be withdrawn.

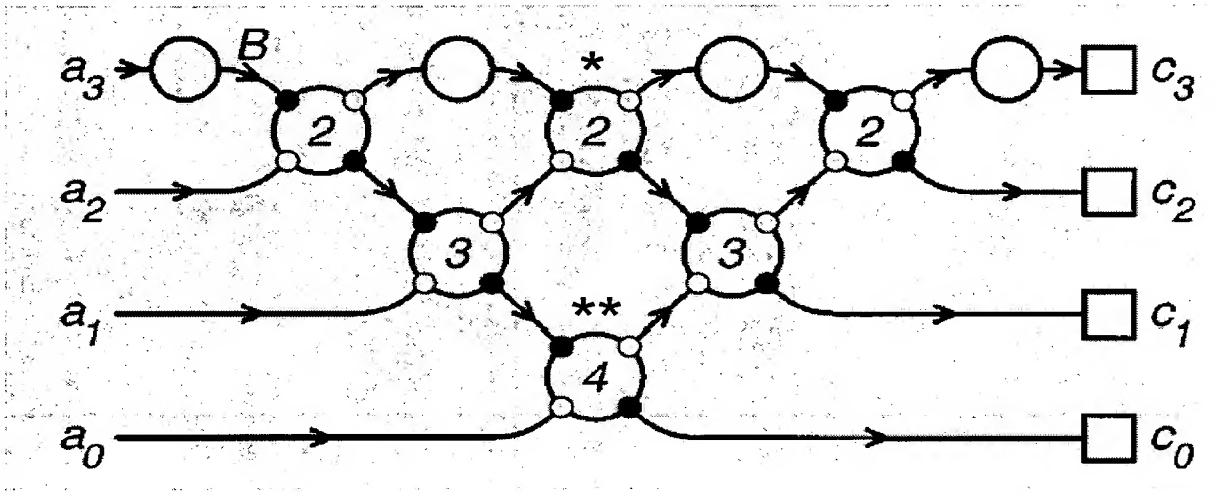
THE 35 U.S.C. § 102(a) REJECTION OF CLAIMS 1 AND 5 SHOULD BE WITHDRAWN

The Examiner has rejected claims 1 and 5 as being anticipated by Saito. The Examiner states that Saito teaches constructing a second series of operations from a first series of operations by changing an execution order of the operations that naturally commute. This is not the case. The Examiner relies on Fig. 2 of Saito for teaching the construction of a second series of operations based upon a first series of operations. Applicant respectfully believes that the Examiner has misinterpreted Fig. 2 of Saito. Fig. 2b of Saito is not a derivation of Fig. 2a of Saito and Fig. 2c is not a derivation of Fig. 2b or Fig. 2a of Saito. Figs. 2a, 2b, 2c, taken together, are the quantum circuits of a five qubit quantum Fourier transform. In other words, the output of Fig. 2a is the input to Fig. 2b and the output of Fig. 2b is the input to Fig. 2c. Put another way, Fig. 2b is a series of operations that sequentially follows the series of operations in Fig. 2a. Fig. 2c is a series of operations that sequentially follows the series of operations of Fig. 2b. Thus, it is not possible for Fig. 2 of Saito to teach the changing of the execution order of operations that mutually commute because Fig. 2 is a single series of operations, not three separate series of operations. Therefore Saito does not teach each and every element of claims 1 and 5 and Applicant respectfully requests that the 35 U.S.C § 102 rejection of claims 1 and 5 be withdrawn.

THE 35 U.S.C. § 102(b) REJECTION OF CLAIM 6 SHOULD BE WITHDRAWN

The Examiner has rejected claim 6 as being anticipated by Griffiths. The Examiner alleges that Griffiths discloses a method for performing a swap operation from a sequence of operations (the operations "2" and "3" on the left side of Fig. 1 of Griffiths); and simultaneously performing two of the operations (the operations "2" and

"4" in the middle of Fig. 1 of Griffiths) that naturally commute. This is not the case. Griffiths does not teach or suggest the simultaneous execution of two operations that naturally commute. For example, the operations "2" and "4" in the middle of Griffiths' Fig. 1 are not executed simultaneously. In fact, Griffiths' Fig. 1 is not a timing diagram. Rather, it is an arrangement of gates that carry out a discrete Fourier transform. Therefore, when a quantum gate is shown directly above or below another gate in Griffiths' Fig. 1, it in no way implies that the two vertically arranged gates are executed simultaneously. For the Examiner's convenience, Fig. 1 of Griffiths is reproduced below.



Conversion of Griffiths' Fig. 1 to a timing diagram in accordance with the conventions of Saito and the pending application gives:

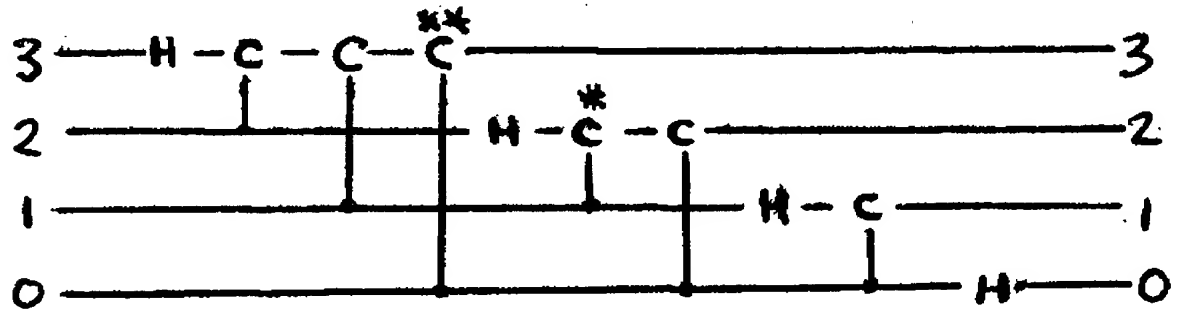


FIG. 1'

The gates * and ** in Fig. 1N correspond to gates in reproduced Griffiths' Fig. 1 that bear the same marks. As can be seen in the timing diagram that corresponds to Griffiths' Fig. 1, gates "2" and "4" are performed at different time intervals, not simultaneously as suggested by the Examiner.

Pending claim 6 recites two operations in a plurality of operations commute and that are performed simultaneously. Griffiths does not disclose such a feature. Accordingly, Applicant requests that the 35 U.S.C § 102 rejection of claim 6 be withdrawn.

THE 35 U.S.C. § 103 REJECTION OF CLAIMS 2-4 AND 7-10 SHOULD BE WITHDRAWN

The Examiner has rejected claims 2-4 as being rejected under 35 U.S.C. § 103(a) as being unpatentable over Griffiths in view of Saito. The Examiner bases this rejection on the premise that Saito teaches changing execution order of operations. However, as discussed in the Applicant's response to the 102 rejections above, Saito does not teach or suggest the changing of the execution order of operations. Griffiths does not remedy this deficiency in Saito. Therefore, the 35 U.S.C. § 103(a) rejection of claims 2-4 should be withdrawn.

The Examiner has rejected claims 7-10 as being rejected under 35 U.S.C. § 103(a) as being unpatentable over Griffiths in view of paragraph 36 of Applicant's specification. The Examiner bases this rejection on the premise that Griffiths discloses two operations in a plurality of operations that commute and are performed simultaneously. However, as discussed in the Applicant's response to the 102 rejections above, Griffiths does not teach or suggest such a feature. Therefore, the 35 U.S.C. § 103(a) rejection of claims 7-10 should be withdrawn.

CONCLUSION

Applicant respectfully requests that the above-mentioned amendments and remarks be entered and made of record in the file history of the subject application. It is believed that all claims are fully allowable and early indication of the same is earnestly sought.

It is believed that no fees are due in connection with the filing of this amendment other than the extension of time and fees for additional claims. However, should the Unites States Patent and Trademark Office determine otherwise, please charge the required fee to Jones Day deposit account no. 50-3013, referencing CAM No. 706700-999107.

Respectfully submitted,

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